IWLS 2005 Benchmarks

Christoph Albrecht
(calb@cadence.com)
Cadence Berkeley Labs

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Outline

- Benchmarks
  - 84 designs with up to 185,000 registers and 900,000 cells collected from different websites
- OpenAccess
  - Open source design database for EDA
- OA Gear
  - An open source library of essential utilities / components built on top of OpenAccess
  - OA Gear Timer: Timing analysis with accurate slew propagation.

Benchmarks

- 84 benchmarks from
  - OpenCores (26)
  - Gaisler Research (4)
  - Faraday Technology Corporation (3)
  - ITC 99 (21)
  - ISCAS 85 and 89 (30)
- All benchmarks synthesized and mapped to a 180 nm library
- In two formats: Verilog and OpenAccess

OpenCores Benchmarks

- OpenCores:
  - Loose collection of people who are interested in developing hardware, with a similar ethos to the free software movement
  - Current emphasis on digital modules called ‘cores’
- 26 different designs (still more on the website)
- http://www.opencores.org

name	function
pci_conf_cyc_addr_dec	PCI
steppermotordrive	Stepper Motor Drive
ss_pcm	Single Slot PCM Interface
usb_phy	USB 1.1 PHY
sasc	Simple Asynchronous Serial Controller
simple_spi	MC68HC11E based SPI interface
i2c	WISHBONE revB.2 compliant I2C Master controller
pci_spoci_ctrl	PCI
des_area	DES optimized for area
spi	SPI IP
systemcdes	SystemC DES
wb_dma	WISHBONE DMA/Bridge IP Core

name	function
des3_area	Tripe DES optimized for performance
tv80	TV80 8-Bit Microprocessor Core
systemcaes	SystemC AES
mem_ctrl	WISHBONE Memory Controller
ac97_ctrl	WISHBONE AC 97 Controller
usb_funct	USB function core
pci_bridge32	PCI
aes_core	AES Cipher
wb_conmax	WISHBONE Conmax IP Core
ethernet	Ethernet IP core
des_perf	DES optimized for performance
vga_lcd	WISHBONE rev.B2 compliant Enhanced VGA/LCD Controller

OpenCores Benchmarks

design	sequential	inverter	buffer	logic	tristate	total
pci_conf_cyc_addr_dec	-	14	1	82	-	97
steppermotordrive	25	68	4	129	-	226
ss_pcm	87	102	3	278	-	470
usb_phy	98	118	17	313	-	546
sasc	117	79	7	346	-	549
simple_spi	132	143	8	538	-	821
i2c	128	211	45	758	-	1,142
pci_spoci_ctrl	60	260	34	913	-	1,267
des_area	64	851	92	2,125	-	3,132
spi	229	462	49	2,487	-	3,227
systemcdes	190	832	136	2,164	-	3,322
wb_dma	563	516	38	2,272	-	3,389
des3_area	128	1,135	142	3,476	-	4,881
tv80	359	1,101	97	5,604	-	7,161
systemcaes	670	786	66	6,437	-	7,959
mem_ctrl	1,083	1,462	221	8,674	-	11,440
ac97_ctrl	2,199	1,525	111	8,020	-	11,855
usb_funct	1,746	1,865	33	9,164	-	12,808
pci_bridge32	3,359	3,095	100	10,262	-	16,816
aes_core	530	5,589	274	14,402	-	20,795
wb_conmax	770	3,366	86	24,812	-	29,034
ethernet	10,544	3,404	234	32,557	32	46,771
des_perf	8,808	28,372	1,489	59,672	-	98,341
vga_lcd	17,079	21,397	2,542	83,013	-	124,031

Gaisler Research Benchmarks

- Gaisler Research:
  - Digital hardware design (ASIC/FPGA) for both commercial and aerospace applications
- http://www.gaisler.com
- LEON2 processor
  - developed for and by the European Space Agency (ESA)
- LEON3 processor
  - 32-bit processor compliant with SPARC V8 architecture

design	sequential	inverter	buffer	logic	tristate	total
leon2	149,381	104,393	14,964	511,665	53	780,456
netcard	97,831	61,712	11,946	552,506	48	724,043
leon3mp	108,839	87,122	3,303	346,539	33	545,836
leon3-avnet-3s1500	185,025	169,668	4,333	540,522	84	899,632

Faraday Benchmarks

- Faraday Technology Corporation
  - http://www.faraday-tech.com/StructuredASIC/download.html
- Three functional blocks:
  - DSP: 16-bit digital signal processor (DSP) with SRAM blocks
  - RISC: 32-bit RISC CPU
  - DMA: Direct Memory Access (DMA) Controller

design	sequential	inverter	buffer	logic	unresolved	total
DMA	2,192	2,678	253	13,995	-	19,118
DSP	3,611	5,258	42	23,523	2	32,436
RISC	7,599	7,370	126	44,872	7	59,974

ITC'99 Benchmarks

- Politecnico di Torino: Fulvio Corno, Matteo Sonze Reorda, Giovanni Squillero
- http://www.cad.polito.it/tools/itc99.html
- 22 designs

Name	Original Functionality
b01	FSM that compares serial flows
b02	FSM that recognizes BCD numbers
b03	Resource arbiter
b04	Compute min and max
b05	Elaborate the contents of a memory
b06	Interrupt handler
b07	Count points on a straight line
b08	Find inclusions in sequences of numbers
b09	Serial to serial converter
b10	Voting system
b11	Scramble string with variable cipher

Name	Original Functionality
b12	1-player game (guess a sequence)
b13	Interface to meteo sensors
b14	Viper processor (subset)
b15	80386 processor (subset)
b16	Hard to initialize circuit (parametric)
b17	Three copies of b15
b18	Two copies of b14 and two of b17
b19	Two copies of b14 and two of b17
b20	A copy of b14 and a modified version of b14
b21	Two copies of b14
b22	A copy of b14 and two modified versions of b14

ITC'99 Benchmarks

design	sequential	inverter	buffer	logic	total
b01	5	27	3	51	86
b02	4	14	2	25	45
b03	30	82	2	271	385
b04	66	257	21	537	881
b05	34	228	33	726	1,021
b06	9	33	1	43	86
b07	49	177	20	492	738
b08	21	59	4	143	227
b09	28	58	4	170	260
b10	17	75	9	210	311
b11	31	178	32	564	805
b12	121	411	73	1,412	2,017
b13	53	92	4	253	402
b14_1	245	1,557	218	6,696	8,716
b14	245	1,518	188	6,728	8,679
b15_1	449	1,565	149	10,295	12,458
b15	449	1,569	201	10,343	12,562
b17_1	1,415	4,627	368	30,973	37,383
b17	1,415	4,564	319	30,819	37,117
b18_1	3,296	11,332	422	76,616	91,666
b18	3,296	11,429	407	76,916	92,048
b19_1	6,594	20,812	531	146,582	174,519
b19	6,594	20,866	439	146,258	174,157
b20_1	490	3,303	289	15,049	19,131
b20	490	3,537	332	14,748	19,107
b21_1	490	3,189	325	14,554	18,558
b21	490	3,392	334	14,502	18,718
b22_1	703	4,767	511	22,147	28,128
b22	703	5,131	390	22,093	28,317

ISCAS Benchmarks

- ISCAS 85 and 89
- http://www.cbl.nscu.edu

design	sequential	inverter	buffer	logic	total
s27	3	7	-	9	19
s208_1	8	17	3	45	73
s349	15	29	9	70	123
s344	15	36	5	76	132
s298	14	34	7	86	141
s382	21	44	2	92	159
s444	21	47	2	92	162
s400	21	41	6	95	163
s386	6	50	6	105	167
s420_1	16	48	13	110	187
s713	19	52	6	115	192
s641	19	48	6	120	193
s526n	21	56	8	143	228
s526	21	74	7	135	237
s510	6	67	21	162	256
s832	5	83	10	235	333
s820	5	98	18	230	351
s838_1	32	90	21	224	367
s1196	18	105	27	333	483
s1238	18	139	46	383	586
s1423	74	121	12	400	607
s1488	6	176	26	428	636
s1494	6	172	23	442	643
s15850	165	130	21	369	685
s9234_1	145	227	4	598	974
s13207	333	168	49	669	1,219
s5378	163	265	31	835	1,294
s38584	1,178	1,017	134	4,395	6,724
s35932	1,728	495	88	4,962	7,273
s38417	1,564	1,300	85	5,329	8,278

Library

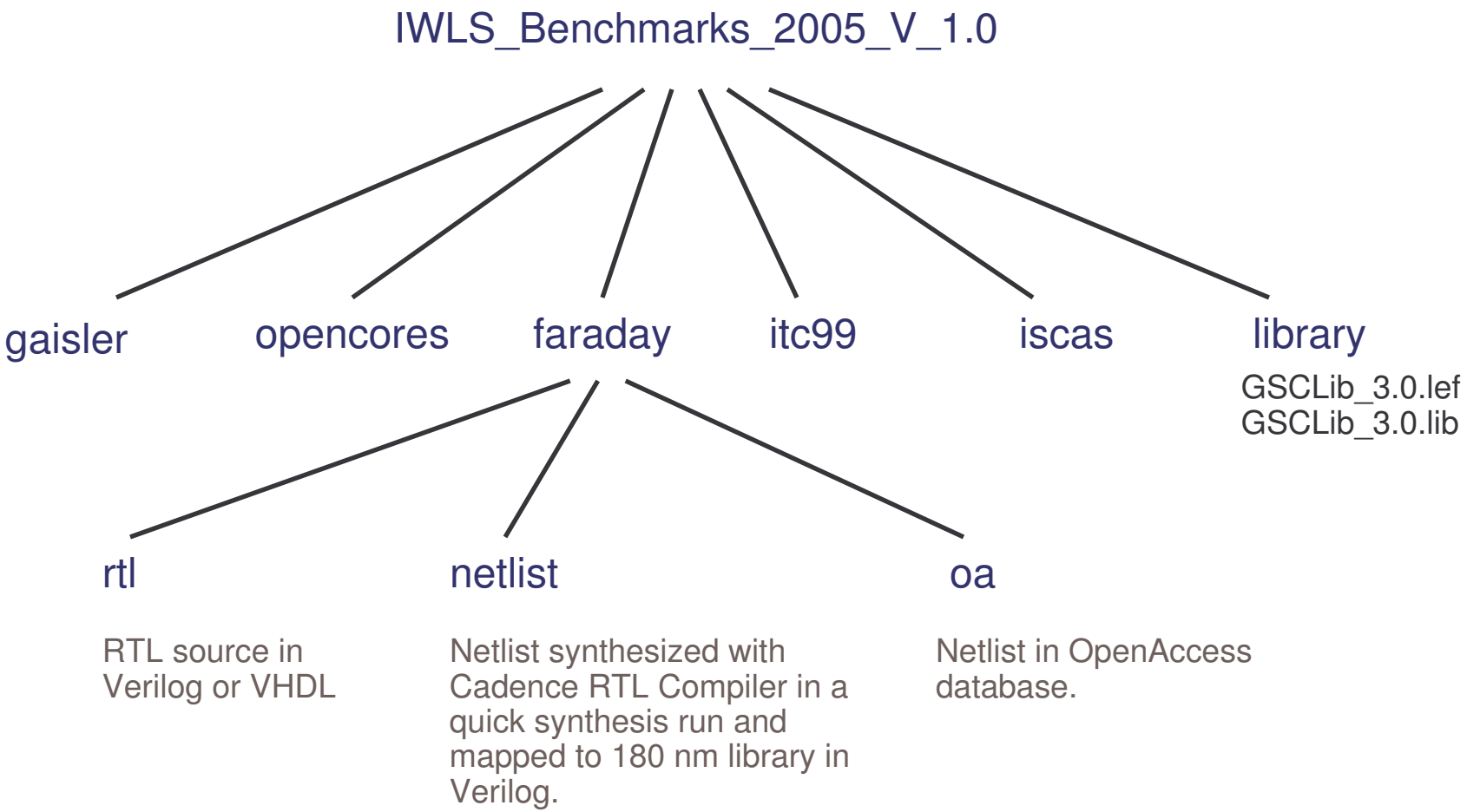
- 180 nm library
- available from Cadence University at

  http://crete.cadence.com

- free for personal or classroom use

INVX1	BUFX1	NOR2X1	OR2X1	OAI21X1	ADDHX1	DFFSRX1
INVX2	BUFX3	NOR3X1	OR4X1	OAI22X1	ADDFX1	DFFX1
INVX4		NOR4X1		OAI33X1		SDFFSRX1
INVX8	CLKBUFX1		AND2X1		TLATSRX1	
	CLKBUFX2	NAND2X1		AOI21X1	TLATX1	
TINVX1	CLKBUFX3	NAND2X2		AOI22X1		
		NAND3X1			XOR2X1	
	TBUFX1	NAND4X1		MX2X1		
	TBUFX2					
	TBUFX4					
	TBUFX8					

Directory Structure



OpenAccess

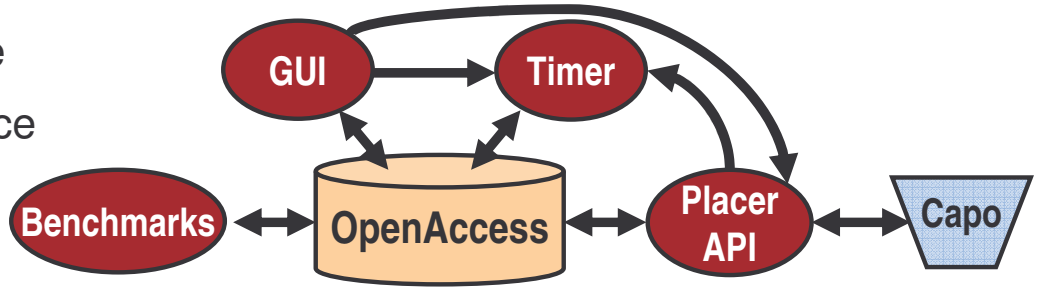
- OpenAccess is an open source design database for EDA
  - OA has been adopted by many companies
  - Standardization helps tool interoperability

- OpenAccess should also be beneficial for academic users
  - Ensures benchmarks, experimental results can be easily exchanged
  - Technology transfer of algorithms developed at universities into industry tools

http://www.si2.org

OA Gear

- OA Gear is a library of essential utilities / components built on top of OpenAccess
  - OA Gear Timer: Full static timer
  - OA Gear Bazaar: User Interface
  - Capo Wrapper: Placer Interface



- Initially released Nov 2004, ~300 downloads so far
- Open source licensing model
  - Critical for academic use, true community development model
  - Working well: Fixes / improvements from user feedback, users have even provided complete bug patches
- Freely distributed, no cost
  - Available even on tightest budget, also free for commercial use

OA Gear Timer

- Timing is often ignored in academic research
  - Difficult/expensive to integrate commercial timing engines
  - Significant task to write own timer
  - Significant calibration/fidelity issues
- Solution: OA Gear Timer
  - Common timing infrastructure
  - Validated, integrated, rich feature set
- Upside
  - Helps ensure results from different researchers can be directly compared

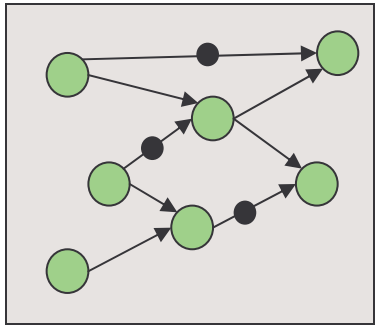
OA Gear Timer

- Supports Cadence .TLF and Synopsys Liberty (.LIB) formats
- Supports .SDC constraint subset
  - Clock period, external delay information
- Incremental Timing Analysis
- Three wire load models (so far…)
  - **Idealized:** ignores wire loads
  - **Linear:** half-perimeter bbox using unit C, R info from technology library
  - **Custom:** allows users to specify their own models for wiring
- Standard APIs & reporting formats
  - The critical path
  - Paths *–from –to –through* a node

OA Gear Future Plans

- Timer:
  - Multiple clocks
  - Latches
  - Multi cycle paths
  - Tristates
  - Statistical Timing Analysis

- Functional Layer
  - And-Inverter Graph extraction: User can attach a reasoning engine of his choice (BDDs, SAT, etc) through a callback interface.
  - Boolean Reasoning
  - Infrastructure for Logic Synthesis



OA Gear: Credits / Website

• Zhong Xiu	Carnegie Mellon	Timer, Warp
• David Papa	Univ. of Michigan	Bazaar, Capo Wrapper
• Afshin Abdollahi	Univ. of Southern California	Timer
• Aaron Hurst	Univ. of California, Berkeley	Functional Layer
• Philip Chong	Cadence Berkeley Labs	OA Gear
• Christoph Albrecht	Cadence Berkeley Labs	OA Gear
• Andreas Kuehlmann	Cadence Berkeley Labs	OA Gear
• Rob A. Rutenbar	Carnegie Mellon	Warp
• Igor L. Markov	Univ. of Michigan	Capo

http://openedatools.si2.org/oagear/